# FreeRTOS DEV API - Extension Interface and MOS issues Analysis

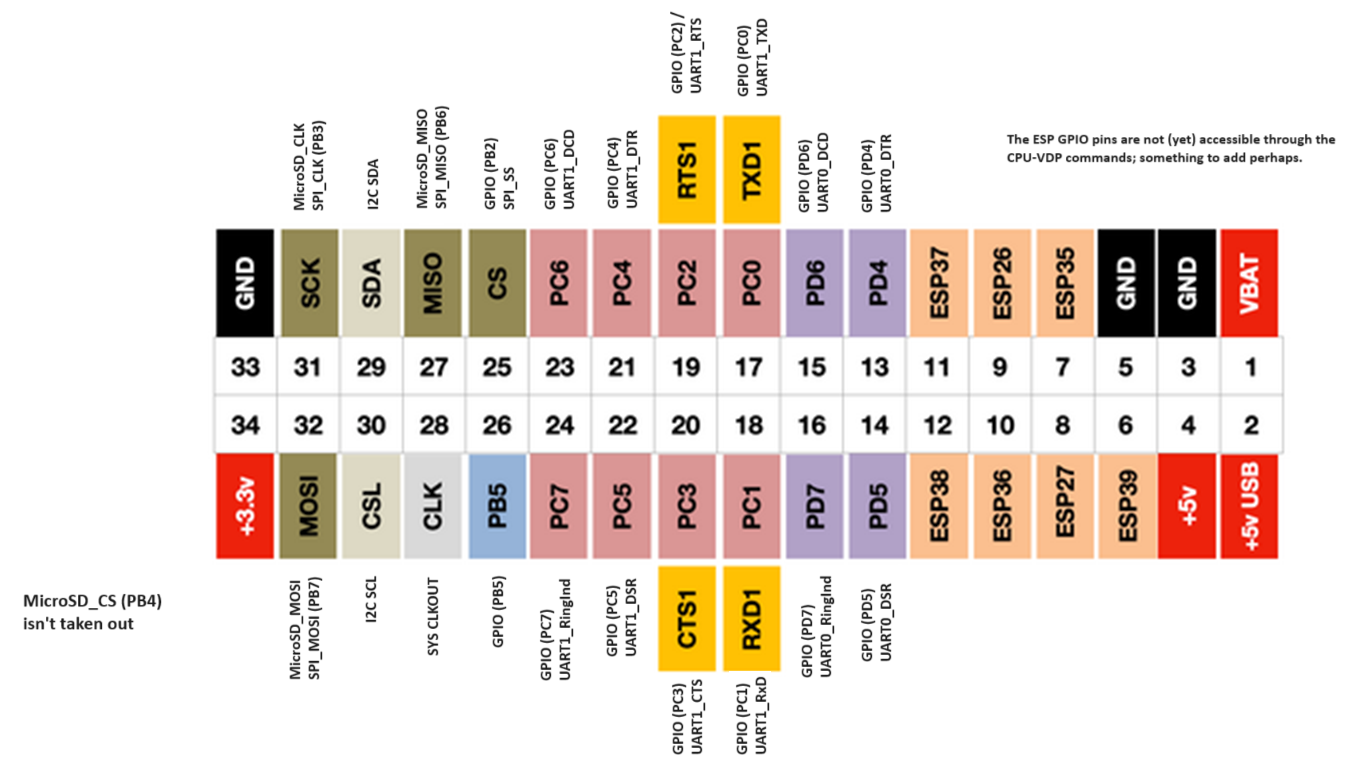
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## Summary

The goal of the FreeRTOS DEV API is to develop a uniform method for programmers to access the Agon Light (and compatibles) hardware Extension Interface, while using as much as possible of the existing ROM-based MOS services[[1]](#footnote-1). The hardware interfaces accessible are I2C, GPIO, SPI and UART. The Agon hardware platforms have no issues, and fully support these interfaces as per the eZ80 capability. However, the MOS software does have issues and use-case limitations, common to both the current Quark (MOS 1.04) and Console8 (MOS 2.x.y) software, that need addressing to meet our goal.

## Extension Interface

The Agon Light, Origins, and Olimex Light 2 (depicted) Extensions Interface are compatible for DEV API.



Refer to <https://agonconsole8.github.io/agon-docs/GPIO/>. The DEV API shall address functions at PD4-PD7, PC0-PC7, CS[[2]](#footnote-2), PB5, MISO, SDA, CSL, SCK, and MOSI. DEV API shall not address any of the remaining pin functions. Platform pinout differences are outlined: Agon Origins 34-pin pin 1 (VBAT) is not connected, but is otherwise an alike pinout; Agon Light has a 32-pin connector, without VBAT and 5v outputs[[3]](#footnote-3), but is otherwise alike; the Console8 40-pin pinout differs more significantly; but all platforms are sufficiently compatible such that just one version of the FreeRTOS DEV API software will run on all of them.

## DEV API outline and MOS Issues

We outline designs for the FreeRTOS DEV API and highlight issues with the MOS software for each of the functional groups in turn. Each functional group (I2C, GPIO, SPI and UART) shall have a unique major number identifying it in the DEV API software. Individual devices shall have a unique minor number.

### GPIO

The MOS API does not expose any GPIO functions. With safeguarding configured, and on application call to Open a device, the FreeRTOS DEV API software shall check that the requested pin(s) have not been previously allocated prior to successfully allocating the GPIO function. Each GPIO pin may be opened as an independent device, with the minor number distinguishing it. Minor numbers shall be assigned as per the pin numbers; for example, device at PB5 shall be GPIO minor device 26. Note that GPIO 25, PB2 (alternately SPI /SS) cannot be assigned to GPIO because of issues in the MOS SPI software (see below). The remaining 13 GPIO-alternate pins (13..16, 17..24, and 26) can be assigned.

#### MOS GPIO Issues

The reset default for all GPIO pins is Mode 2 = Input with interrupts disabled. The MOS file src/gpio.asm contains one public function, GPIOB\_SETMODE to set the mode of port B. This is called once from src\_startup/init\_params\_f92.asm (modified version of the Zilog startup), to configure Port B2 (GPIO 25 / SPI SS) as Mode 9 (as per PS015317 table 6, as a Rising Edge interrupt input). This may be a left-over from testing MOS SPI. Note also the bug in src/gpio.asm:GPIOB\_SETMODE::GPIOB\_M4 dual edge interrupt, should be clear DDR, clear ALT1, set ALT2; although that mode is unused.

#### DEV API GPIO

There is no MOS API for programmers to invoke GPIO functions. The FreeRTOS DEV API shall craft new software. There are numerous examples of setting up GPIO registers in the MOS software to build on.

#### GPIO Errata – Edge-driven interrupts

Bug: Refer to Zilog UP0049 item no.6, “GPIO edge-trigger interrupt mapping error”. Use of *edge-driven* interrupts (modes 6 and 9) are limited due to a bug in the chip logic. In particular, interrupt clear down will not work correctly for certain combinations of GPIO and alternate function pin assignment within any given port.

Resolution: To achieve proper interrupt clear down behaviour for a particular port pin, its mirror pin must be programmed in a similar manner (i.e. edge-driven interrupt). For any port, for any pin, its mirror pin = 7 - pin#; giving the mirror pin pairs {(7,0),(6,1),(5,2),(4,3)}.

Impact for Agon Light2 at Extension Interface:

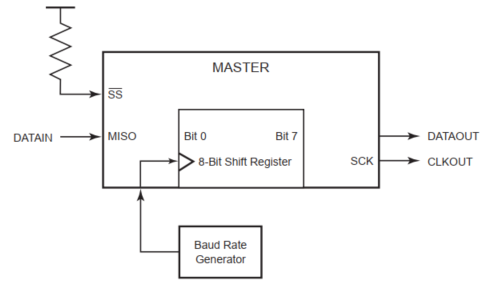
|  |  |  |
| --- | --- | --- |
| Port / Pin | Mirror → Function | Notes |
| PD7 | PD0 → Uart0 TX | Tested using PD7 in DEV\_MODE\_GPIO\_INTRDE with PD4 DEV\_MODE\_GPIO\_OUT. PD7 falling edge events are captured and cleared. PD7 rising edge events are not captured. No resolution as UART0 is the eZ80-VDP link. |
| PD6 | PD1 → Uart0 RX | Tested similar to PD7. PD6 rising edge events are not captured. PD6 falling edge detections only. |
| PD5 | PD2 → Uart0 RTS | Tested similar to PD7. PD5 rising edge events are not captured. PD5 falling edge detections only. |
| PD4 | PD3 → Uart0 CTS | Tested using PD4 configured as DEV\_MODE\_GPIO\_INTRDE with PD5 DEV\_MODE\_GPIO\_OUT. PD4 Rising edge events are not captured. PD4 Falling edge detections only. |
| PC7 | PC0 → Uart1 TX | Similar to PD7 iff UART1 is used simultaneously in DEV\_MODE\_UART\_MODEM\_FLOWCTRL. Tested using PC7 in DEV\_MODE\_GPIO\_INTRDE with PD4 DEV\_MODE\_GPIO\_OUT. Both PC7 rising and falling are captured. |
| PC6 | PC1 → Uart1 RX | Similar to PD6 iff UART1 is used simultaneously in DEV\_MODE\_UART\_MODEM\_FLOWCTRL; should be okay otherwise. Not yet tested. |
| PC5 | PC2 → Uart1 RTS | Similar to PD5 iff UART1 is used simultaneously in DEV\_MODE\_UART\_MODEM\_FLOWCTRL; should be okay otherwise. Not yet tested. |
| PC4 | PC3 → Uart1 CTS | Similar to PD4 iff UART1 is used simultaneously in DEV\_MODE\_UART\_MODEM\_FLOWCTRL; should be okay otherwise. Not yet tested. |
| PC3 | PC4 → Uart1 DTR | Similar to PD3 iff UART1 is used simultaneously in DEV\_MODE\_UART\_HW\_FLOWCTRL; should be okay otherwise. Not yet tested. |
| PC2 | PC5 → Uart1 DSR | Similar to PD2 iff UART1 is used simultaneously in DEV\_MODE\_UART\_HW\_FLOWCTRL; should be okay otherwise. Not yet tested. |
| PC1 | PC6 → Uart1 DCD | Similar to PD1 iff UART1 is used simultaneously; should be okay otherwise. Both PC7 rising and falling are captured. |
| PC0 | PC7 → Uart1 RI | Similar to PD0 iff UART1 is used simultaneously; should be okay otherwise. Not yet tested. |
| PB5 | PB2 → SPI SS | As PB2 is a constant level, it will impact interrupts on PB5. Tested using PB5 configured as DEV\_MODE\_GPIO\_INTRDE with PD4 DEV\_MODE\_GPIO\_OUT. PB5 rising edge events are not captured. PB5 falling edge detections only. |
| PB2 | PB5 → GPIO | We can’t use PB2 (pin 25) for GPIO due to MOS SPI software issues |

### SPI

The MOS API does not expose any SPI functions. On application invocation, the FreeRTOS DEV API shall check that a requested (/SS emulation) pin is not allocated prior to successfully allocating the SPI device. Each SPI slave device shall be uniquely distinguished with a minor number. Minor numbers shall be as per the pin number assigned as /SS; for example, device with /SS assigned to PB5 shall be SPI device 26.

#### MOS SPI Issues

MOS main.c calls src/spi.asm::\_init\_spi to setup the SD-card interface. The comment “SS must remain high for SPI to work properly” is clarified with reference to PS015317 fig 29 eZ80 SPI as a Master Device:



The sole SPI Master device is responsible for generating the clock signal, SCK, in all data exchanges.

MOS \_init\_spi re-configures PB2 to GPIO Mode 1 (as per PS015317 table 6, a GPIO-controlled constant ‘1’ output). (It then does similar for PB4, which is the SD-card /CS, to de-select the SD-card.) This PB2 configuration fixes the eZ80 as the SPI master. (As the MOS 1.04 software stands, PB2 will output a continuous ‘1’ value once SPI is initialised. We can observe this with a scope or multimeter.)

#### DEV API SPI

With PB2/SS fixed high, DEV API shall allocate other GPIO pins (e.g. pin 26, PB5) to emulate /SS (normally high, asserted low). Each emulated /SS pin shall be designated with a unique minor number as per its pin number - for example, device at PB5 shall be SPI minor device 26. Each SPI device may be opened individually.

##### /SS driving control

PB4 (SD-card /SS) is normally asserted. To ensure SD-card use does not conflict with external SPI device(s) read and write, DEV API shall de-assert the SD-card /SS PB4 (drive it high) prior to asserting an emulated /SS pin (driving it low). And conversely, DEV API shall de-assert an emulated /SS pin (driving it back high) on completion of each I/O operation, before re-asserting the SD-card /SS PB4 (driving it low).

Slave Interrupts (to request a transfer) are not a part of the SPI protocol. The SPI-protocol requires the application software poll the devices attached via the Extensions Interface, to retrieve any data from them. However, independently of DEV API and the SPI protocol, and to facilitate slave request for a SPI data exchange, the application developer can assign a second GPIO pin to generate an interrupt. This interrupt routine could invoke a SPI device read operation.

##### Multiplexing

In a system architecture containing multiple SPI devices, and to make best use of the limited number of /SS emulation pins that can be allocated at the Extension Interface, the Agon user may opt to place a line decoder or fanout IC, e.g. an SN74HC138, in-circuit with external SPI device chip selects. A decoder converts N inputs into 2N outputs (a binary transformation). For example, allowing 3 /SS pins to reach 8 devices. In such a configuration, the user program shall Open three SPI devices with a Group Mode attribute, so that the /SS emulation pins are asserted in a binary 2N format (rather than individually, N) when performing I/O operations.

The total number of devices that can be supported is decided by one of: the number of available GPIO lines that can be assigned to emulate /SS, including any use of Group Mode chip selects; the total electrical load that can be drawn from the whole Agon system[[4]](#footnote-4); the wire distance operating at the Agon SPI clock rate of ≈3MHz (fixed in the MOS software, presumably the maximum rate of the on-board SD-card device).

### UART

The MOS code appears derived from the ‘Poll’ subset of the Zilog uart software base. It facilitates 1 byte at a time poll-mode transceiving. It supports either 2-pin ‘software flow control’ or 4-pin half-duplex ‘hardware flow control’, but not 8-pin full-duplex ‘modem flow control’. It does not make use of the device FIFO interrupt-mode buffer capability. Consequently, poll-mode ties up CPU-time in performing serial data transfer, when it could otherwise spend some of that time multi-tasking. However, that makes the MOS code simpler, and is all that is required for the Uart0 CPU-VDP link in Agon Light.

With Uart0 dedicated to the CPU-VDP link, only one UART minor device 1 is available for FreeRTOS. With safeguarding configured, the FreeRTOS DEV API software shall check that a requested pin has not been allocated prior to successfully allocating the application-requested UART1. The application can open UART1 in one of three modes, that require allocation of different pins: NO\_HW\_FLOWCONTROL (also known as software flow control), which requires pins 17 and 18 only; HW\_FLOWCONTROL, or half-duplex, which requires pins 19 and 20 in addition; and MODEM\_FLOWCONTROL, or full-duplex, which further requires pins 21 through 24.

The first two modes are sufficient between point-to-point connected DTEs (data terminal equipment, or computers such as the CPU to VDP) over short distances. Data rates decrease with distance due to signalling capacitance and noise. Modem flow control enables connection over longer distances via DCE (data communication equipment[[5]](#footnote-5)) using (higher-power) signal carrier technology. This mode generalises the ability of the controller (CPU) to act as a micro-controller of remote end equipment. It also enables full duplex (simultaneous tx and rx) between peer-to-peer micro-controllers.

#### MOS UART Issues

There’s a bug in src/serial.asm:UART1\_serial\_GETCH::189, such that it tests whether UART0 is enabled rather than UART1. An outcome is that if an application calls mos\_api\_ugetc when no external device is connected to UART1, then the application will busy wait evermore; needing a hardware reset.

#### DEV API UART

DEV API shall provide new software that will use the eZ80 UART device with FIFO buffers in interrupt mode. It shall provide the ability to operate in half- or full-duplex transmission, using software-, hardware-, null-modem- or full-modem signalling.

The API shall allow either buffered or non-buffered methods for application calling, either of which allow other tasks to run concurrently. In non-buffered mode the calling task will be blocked until either transmission is complete or an error occurs. This mode is best used with a software task dedicated to uart i/o. Whereas in buffered mode the calling task will not be blocked, but continue to run concurrently with uart transmission. This mode is best used with a task design that loops around a number of independent activities.

### I2C

The MOS API provides functions to support an I2C bus in Single Master mode only (akin to SPI single mastering). With safeguarding configured, the FreeRTOS DEV API software shall check that the device has not been allocated prior to successfully allocating it.

The eZ80 I2C device operates from dedicated pins (with no alternate functions). Only one I2C device is available, minor number 0.

#### MOS I2C Issues

The MOS I2C implements Single Mastering, through Master Transmit and Master Receive modes for writing and reading devices respectively[[6]](#footnote-6); but omits the Slave Receive and Transmit (Slave Addressed) modes, for responding to another bus master. This limits the Agon capability as a Micro-Controller to inter-network.

The MOS I2C software implements 7-bit addressing only; it does not implement 10-bit extended addressing[[7]](#footnote-7). With 16 reserved 7-bit address numbers, this may be a problem if: the number of attached devices exceeds 112, which use-case seems rare – but e.g. Christmas tree LEDs; or if an application-specific sub-netting address scheme is to be used, exhausting the logical assignment of minor numbers; or if certain devices only support 10-bit addressing (e.g. on 7-bit address assigned numbers exhaustion – see <https://learn.adafruit.com/i2c-addresses/the-list> for example).

#### DEV API I2C

One use-case for I2C Slave modes (bus multi-mastering) is Agon peer-to-peer networking. Presently, the ability to natively inter-connecting Agon devices is limited[[8]](#footnote-8). I2C is a true multi-master bus, providing arbitration and collision detection, and presents the best way of doing that. With the addition of Slave-addressed read and write modes, and corresponding interrupt support, we might be able to realise an Agon Cluster!

## Solution Options

As much as possible we want to locate software in ROM, to keep the RAM footprint to a minimum. Where we need to use RAM, that use should be user-configurable.

### ROM – modify MOS

We could fork and extend the MOS Quark software to produce a new release, 1.05 (or maybe 1.1.0 as a new and distinct branch of MOS): fix the UART1 bug; finish the I2C software with multi-mastering, to include slave-addressed modes and status register cases; fix the GPIOB\_SETMODE bug, add new GPIO code and extend the MOS API accordingly; add new SPI code, extending the MOS API.

The latest Console8 MOS version can merge the changes in straight-forwardly.

There is much merit in this option. But we will have failed on ‘needs no re-FLASHing’ of the firmware to work. Maybe more than once if we introduce bugs. And personally, I don’t have a working Acclaim! Smart Cable hardware debugger yet (device driver problem); which will probably be needed.

### RAM – extend DEV API

We can create the DEV API as outlined above. The additional SPI software is feasible, although duplication of read and write functions is less desirable. If we omit Modem Flow Control until it is specifically requested, and at ≈250 lines of code, replacing UART code should be straight-forward and small enough. The GPIO is wholly new, but should be modest enough to make a configurable build-option acceptable. I2C will be the biggest re-implementation – but either the (Single Master) I2C MOS or (Multi-Master) DEV API methods can be user-selected through configuration.

Any bugs we introduce with this solution are easily fixed, without needing yet another candidate release version of MOS. The MOS software can inherit the bug fixes from DEV API at a later date with no impact on FreeRTOS applications.

## References

<https://agonconsole8.github.io/agon-docs/GPIO/> Outline of Agon Extension Interface (so-called GPIO). Note error on pins 29,30 on the Agon Light pinout. Note the ending textual error, should read ‘go via a “transducer”’ and not a “transputer”.

<https://www.nxp.com/docs/en/user-guide/UM10204.pdf> I2C-bus specification and user manual

<https://learn.adafruit.com/i2c-addresses/the-list> Partial list of assigned 7-bit I2C addresses as an example. See also <https://i2cdevices.org/addresses>.

<https://www.analog.com/media/en/technical-documentation/app-notes/an-1248.pdf> SPI application note, outlining a number of potential implementation incompatibilities.

<https://www.mouser.com/datasheet/2/450/up0049-21068.pdf> Zilog eZ80F92 chip errata. (Also in ZDSII\_eZ80Acclaim!\_5.3.5\Documentation\Errata\.) Especially item no. 6 on edge-driven interrupts. And item no.7 on continuous uart Rx interrupts in a certain configuration.

<https://application-notes.digchip.com/003/3-5557.pdf> Maxim review of RS-232 UART operation.

<http://www.nullmodem.com/NullModem.htm> Null-modem wiring, for connecting two UART DTEs directly (without DCEs). See also: <https://en.wikipedia.org/wiki/Null_modem#Wiring_diagrams>

1. Using FreeRTOS ‘requires no re-FLASHing’ – you just build a MOS application, load and run it. [↑](#footnote-ref-1)
2. DEV API cannot control CS due to MOS software limitations, discussed below. [↑](#footnote-ref-2)
3. All platforms Extension Interfaces (I2C, GPIO, SPI and UART) operate at 3.3v peak voltage (wrt GND). [↑](#footnote-ref-3)
4. It would be far better to power external devices independently of Agon, to reduce the current draw – but many users will nonetheless take out the power rail from Agon. [↑](#footnote-ref-4)
5. Nowadays we would use wifi technology instead, with a micro-processor in the wifi device using a simple serial (uart, spi, i2c) handshake between that and our CPU. But if you want the retro experience, then RS232 it is. [↑](#footnote-ref-5)
6. Known as Single Master <https://www.i2c-bus.org/singlemaster/> [↑](#footnote-ref-6)
7. The address domains are mutually exclusive: the 7-bit address 0x1 is distinct from the 10-bit address 0x1 (although a single device could respond to either). [↑](#footnote-ref-7)
8. Something like an external wireless network device can be attached. [↑](#footnote-ref-8)